Discrete-Time Mixing Receiver Architecture for RF-Sampling Software-Defined Radio

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***Abstract*—A discrete-time (DT) mixing architecture for RF-sampling receivers is presented. This architecture makes RF sampling more suitable for software-defined radio (SDR) as it achieves wideband quadrature demodulation and wideband harmonic rejection. The paper consists of two parts. In the first part, different downconversion techniques are classified and compared, leading to the definition of a DT mixing concept. The suitability of CT-mixing and RF-sampling receivers to SDR is also discussed. In the second part, we elaborate the DT-mixing architecture, which can be realized by de-multiplexing. Simulation shows a wideband 90° phase shift between I and Q outputs without systematic channel bandwidth limitation. Oversampling and harmonic rejection relaxes RF pre-filtering and reduces noise and interference folding. A proof-of-concept DT-mixing downconverter has been built in 65 nm CMOS, for 0.2 to 0.9 GHz RF band employing 8-times oversampling. It can reject 2nd to 6th harmonics by 40 dB typically and without systematic channel bandwidth limitation. Without an LNA, it achieves a gain of -0.5 to 2.5 dB, a DSB noise figure of 18 to 20 dB, an IIP3 $= +10$ dBm, and an IIP2 $= +53$ dBm, while consuming less than 19 mW including multiphase clock generation.**

***Index Terms*—Sampling, RF sampling, sampling receiver, oversampling, mixing, discrete-time mixing, continuous-time mixing, software-defined radio, SDR, software radio, SWR, harmonic rejection, anti-aliasing, phase shift, quadrature, demodulation, downconversion, downconverter, de-multiplexing, de-multiplexer, wideband, wideband sampling, receiver, wideband receiver, interference, CMOS, system-on-chip, SoC.**

I. Introduction

RF-SAMPLING receivers have recently drawn both academic [1], [2] and industrial interests [3]–[6]. They sample the signal early in the receiver chain *before or simultaneously with* downconversion, instead of *after* downconversion as done in conventional continuous-time (CT) mixing receivers. Direct RF-sampling provides the potential to move A/D converters (ADC) closer to antenna aiming at software radio (SWR) or software defined radio (SDR). As initially proposed by Mitola [7] and BellSouth [8], the ADC in an ideal SWR operates on the RF signal, while in a (more practical) SDR the ADC may be located at IF, after frequency downconversion, still achieving certain flexibility. Reconfigurability by software should allow it to support different wireless standards in one device, bringing cost and size reductions. SDR might also allow for upgradable radios and cognitive radio (CR), to improve the efficiency of utilizing scarce spectrum resources.

Several CMOS ICs have recently been published with features suitable for SDR receivers. Reference [9] focuses on flexible baseband filters using switched-capacitor circuits and [10] on the programmability of parameters such as gain, noise figure (NF), linearity, and power consumption. Reference [11] proposes techniques to mitigate out-of-band interference with less dedicated RF pre-filtering. All these receivers [9]–[11] use wideband front-ends based on CT mixing. On the other hand, traditional RF sampling [1]–[6] is not directly suitable for SDR [12], as it provides quadrature demodulation and harmonic rejection over a limited channel bandwidth (BW), limiting SDR flexibility.

This paper proposes a discrete-time (DT) mixing architecture [13], featuring *wideband* quadrature mixing for I/Q demodulation and image rejection, and *wideband*[1] harmonic rejection to suppress wideband interference. To verify the concept, we present a downconverter in 65 nm CMOS targeting CR applications in the television broadcasting band [14]. Wideband features can be useful there to exploit free spectrum segments distributed over a wide band in CR applications.

Compared to [13], this paper proposes a way to classify different downconversion techniques to clarify distinctions, and discusses different receiver architectures for SDR. Moreover, it describes the DT mixing concept and circuit implementation in detail, and presents new measurements obtained from packaged chips ([13] used wafer probing). This work focuses on the DT-mixing downconverter, while [15] focuses on the front-end tunable *LC* filter and the LNA.

The classification and comparison of frequency downconversion techniques is described in Section II, showing how DT mixing is different. Section III further explains the DT mixing concept and how it can be used to reduce aliasing. To verify the concept, a specific implementation in 65 nm CMOS is presented in Section IV, followed by Section V discussing the measurement results. Conclusions are drawn in Section VI.

II. Classification and Comparison of Frequency Downconversion Techniques

Different frequency downconversion techniques have been proposed for radio receivers, most notably mixing and sampling. We would like to compare them and answer questions such as: what are the fundamental distinctions among them? Does early sampling in a receiver chain bring additional flexibility? Does sampling suffer more from clock jitter compared to mixing?

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[1]Twice "*wideband*" refers to wide channel bandwidth, while "wideband interference" refers to both the RF and channel bandwidth.

TABLE I
CLASSIFICATION OF FREQUENCY DOWNCONVERSION TECHNIQUES*

Principle \ Input	Analog-CT	Analog-DT	Digital
Mixing (observation rate does not change)	CT Mixing[1]	**DT Mixing[2] (proposed)**	Digital Mixing[3]
Sampling (observation rate does change)	CT-to-DT Sampling[2]	DT Re-sampling[2]	Digital Re-sampling[3]

[1]CT-mixing receiver [2]RF-sampling receiver [3]Ideal SWR receiver

*Based on the type of input signal (continuous/discrete in time/amplitude) and the downconversion principle (mixing/sampling); commonly used receiver names are also indicated by superscripts (see also Fig. 2), showing that RF sampling fits three classes.

To compare downconversion techniques, we propose a classification in Section II-A. This also leads to the definition of the DT-mixing technique, which is the main subject of Sections III to V. Section II-B compares mixing and sampling, stressing their fundamental distinction. Based on the classification, receiver architectures and their suitability for SDR are discussed in Section II-C.

A. Classification of Downconversion Techniques

Table I classifies frequency downconversion techniques in two respects. The columns are defined by the input signal domain, i.e., continuous-time (CT) versus discrete-time (DT) and continuous-amplitude versus discrete-amplitude. This results in three columns: analog-CT (CT and continuous-amplitude), analog-DT (DT and continuous-amplitude), and digital (DT and discrete-amplitude).[2] The rows differ in downconversion principle, i.e., mixing or sampling, where downconversion by sampling is due to aliasing. Thus:

1) For an analog-CT input signal, the downconversion can be realized by either CT mixing or CT-to-DT sampling. Please note that a sampler may or may not do downconversion (aliasing), depending on Nyquist criterion.
2) For an analog-DT input signal, DT mixing but also DT re-sampling can realize downconversion. Note that DT re-sampling has many uses, e.g., decimation by down-sampling or interpolation by up-sampling. Here the purpose is to exploit the aliasing effect associated with re-sampling for frequency conversion.
3) For a digital input signal, downconversion can be done by digital mixing or digital re-sampling.

While all the other five techniques in Table I have been discussed in literature, to the authors' knowledge, we were the first to propose and implement the concept of DT mixing in a receiver [13]. References [1]–[6] apply CT-to-DT sampling for downconversion, while [9]–[11] and [18]–[20] apply CT mixing. DT re-sampling (decimation) has also been used in [1] for a second downconversion.

[2]A column for CT discrete-amplitude signals could also be added, but we omitted it for simplicity and because we are not aware of any radio example operating in this domain, although some work [16], [17] explores the properties of CT DSP systems.

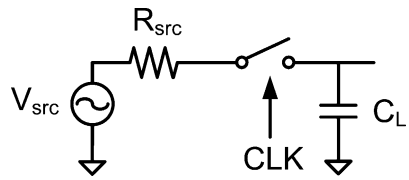

Fig. 1. A general switching system for mixer or sampler.

Sometimes, classification is difficult. For instance, the circuit in Fig. 1 has been presented as a passive mixer[3] [18]–[20] but also as a sampler [1], [2]. The next section discusses mixing and sampling in a bit more detail to assist classification.

B. Fundamental Distinction Between Mixing and Sampling: Observation Rate Changes or Not

Both mixing and sampling are often explained as a multiplication in the time domain or convolution in the frequency domain. However, there is a fundamental distinction, as discussed below. When CT-to-DT sampling is written as a multiplication of a CT input signal $x(t)$ with a Dirac comb $\delta_T(t) = \Sigma\delta(t - n \cdot T_s)$, where n is an integer among $[-\infty, +\infty]$, the sampled signal $x_s(t)$ and its Fourier transform become

$$x_s(t) = x(t) \cdot \delta_T(t) \overset{Fourier}{\leftrightarrow}$$
$$X_s(f) = X(f) \otimes \frac{1}{T_s} \sum_{n=-\infty}^{+\infty} \delta(f - nf_s)$$
$$= \frac{1}{T_s} \sum_{n=-\infty}^{+\infty} X(f - nf_s). \quad (1)$$

where T_s and f_s are the period and the frequency of the sampling clock. $X(f)$ and $X_s(f)$ are Fourier transforms of $x(t)$ and $x_s(t)$ respectively. Equation (1) is commonly used to describe ideal sampling, but the scaling factor $1/T_s$ is often neglected. This scaling factor suggests a "gain" of $1/T_s$ with a unit of "Hz", which seems strange. This issue can be resolved by realizing that (1) is only half of the story. Sampling is more than just multiplication; namely also CT-to-DT conversion.

The signals $x(t), \delta_T(t)$, and $x_s(t)$ are all defined in the CT domain. If we convert $x_s(t)$ into DT-domain as $x_s(k)$ and apply a DT Fourier transform, we get a frequency-domain representation with continuous but normalized frequency axis, i.e., f/f_s. Defining ratio $r = f/f_s$, we can obtain the frequency-domain representation on the r-axis by substituting $f = r \cdot f_s$ into (1):

$$X_s(r \cdot f_s) = X(r \cdot f_s) \otimes \frac{1}{T_s} \sum_{n=-\infty}^{+\infty} \delta(r \cdot f_s - n \cdot f_s)$$
$$= X(r \cdot f_s) \otimes \sum_{n=-\infty}^{+\infty} \delta(r - n). \quad (2)$$

Note that the factor $1/T_s$ disappears in (2), due to the scaling property of the δ-function. If we define $Y_s(r) = X_s(r \cdot f_s)$ and $Y(r) = X(r \cdot f_s)$, then (2) can be written as

$$Y_s(r) = Y(r) \otimes \sum_{n=-\infty}^{+\infty} \delta(r - n) = \sum_{n=-\infty}^{+\infty} Y(r - n). \quad (3)$$

[3]For a current-driven mixer, a resistor in parallel with C_L would be desired to define the voltage conversion gain from RF to baseband. But if the mixer is driven by a voltage source such as in Fig. 1, such a resistor is not necessary.

$Y_s(r)$ is the frequency-domain representation of $x_s(k)$ and $Y(r)$ is equivalent to $X(f)$ but on the r-axis. Comparing (3) to (1), we see that in the *true* DT domain, the scaling farctor $1/T_s$ has disappeared and the gain of an ideal sampler is 1, as expected. Therefore, the step of CT-to-DT conversion is crucial for a sampling operation.

DT signal has a finite "observation rate" (same as sample rate for the DT case) which is inversely proportional to the sampling interval ΔT. For the sake of the classification, a CT signal can be considered as a limiting case of a DT signal with $\Delta T \to 0$, i.e., its "observation rate" goes to infinity. Thus, we can view CT-to-DT conversion as a way to reduce the observation rate from infinite (CT signal) to finite (DT signal) and CT-to-DT sampling nicely fits in one row with DT re-sampling and digital re-sampling (second row of Table I). They sample or re-sample the input signal so to change ΔT between samples and hence the observation rate. In contrast, all the mixing techniques translate the signal frequency but do *not* change ΔT nor the observation rate. For a CT mixer, both input and output signals are continuous in time, i.e., both have an infinite observation rate. For a DT mixer or a digital mixer, the input and the output signals also have the same (finite) observation rate.

This time-domain property can serve as an important distinction between mixing and sampling. For example, for Fig. 1 there is a simple distinction depending on how the output signal is used. If the output signal is used continuously over all time, then the circuit is a CT mixer. However, if the output signal is only evaluated at discrete time points, e.g., only at the end of each LO cycle, then the circuit is a CT-to-DT sampler. Thus, the distinction is *not in the circuit itself but in the way of interpreting/using the output*, i.e., whether the observation rate changes or not from input to output.

Note that we discussed a CT-to-DT sampling above, without "hold effect"[4] which otherwise means a CT output. Therefore, in this paper, we will use the letter "S" as the symbol for sampler but not "S/H".

C. Receiver Architectures for SDR

We will now discuss different ways to implement frequency downconversion in receiver architectures and discuss their suitability to SDR applications. Fig. 2 shows three simplified architectures, each consisting of a mixer, low-pass filter (LPF), sampler (S) and quantizer (Q). Other blocks such as amplifiers and LOs are also important but omitted here for figure clarity. Comparing Fig. 2(a), (b) and (c), the mixer-LPF combination shifts to the right and the sampler/quantizer to the left, representing the trend to move the sampler closer to the receiver input and apply RF-sampling.

Fig. 2(a) shows a traditional CT-mixing receiver with frequency conversion in the CT domain, which is commonly used today for zero-IF or low-IF receivers. In contrast, in Fig. 2(c) frequency conversion is done in the digital domain, *after* both sampling and quantization (A/D conversion). Here either a digital mixer or digital re-sampler can be used for frequency downconversion. This type of receiver fits in the last column of Table I and is indicated as "ideal SWR receiver".

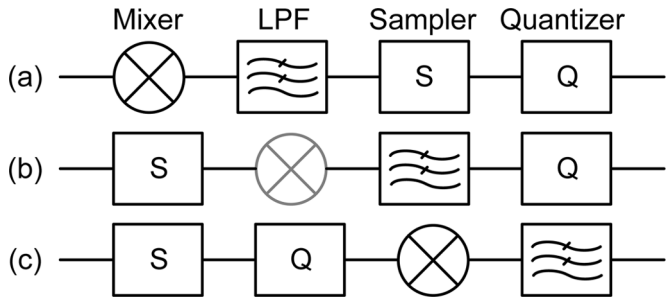

Fig. 2. Three (simplified) receiver architectures: (a) CT-mixing receiver; (b) RF-sampling receiver; (c) ideal software radio (SWR) receiver; showing a trend to move the "mixer-LPF" to the back-end.

Fig. 2(b) shows a sampler followed by a mixer, *in front of* the quantizer. As the CT-to-DT sampler receives RF signals, this architecture is often called an "RF-sampling receiver" in literature. This name includes three sub-classes as shown in Table I. In traditional RF-sampling receivers [1]–[6], the DT mixer in Fig. 2(b) (shown in grey) is missing since the downconversion was realized using the CT-to-DT sampler itself or a following DT re-sampler. Also the ideal SWR receiver samples signal at RF but we do not call it an "RF-sampling receiver" in accordance with literature.

The ideal SWR receiver [Fig. 2(c)] offers maximum flexibility, as it can select and process any band or channel in the digital domain. On the other hand, the CT-to-DT sampler (S) in an ideal SWR receiver does not translate desired signals in frequency, but only does so in the digital domain. Therefore, signal processing requirements are huge and ADC has to convert the full RF-spectrum of interests directly into the digital domain which is usually not feasible [21]. The RF-sampling receivers implemented in [1]–[6] still down-convert and select the desired channel in the analog domain. Therefore, the main asset of an ideal SWR receiver, i.e., flexibility, is *not* inherently shared by RF-sampling receivers. Still, RF-sampling receivers [Fig. 2(b)] as well as CT-mixing receivers [Fig. 2(a)] can be adapted for some degree of flexibility and software control, to make them suitable for SDR applications. However, there is no apparently a priori preference for one of the two.

A common concern for RF-sampling receivers is the clock jitter. It can be shown [22] that the jitter induced error for CT-mixing is proportional to the LO frequency f_{LO}, while for RF-sampling it is proportional to the RF input frequency f_{RF}. For zero-IF or low-IF receivers, f_{LO} and f_{RF} are almost equal, and hence the difference in jitter requirement between CT-mixing and RF-sampling receivers is small [22]. The feasibility of RF-sampling receivers for practical use has been verified by [3]–[6].

Compared to CT-mixing receivers, RF-sampling receivers may require extra complexity, due to RF-related baseband sample rate [12] and extensive clock control for the switched-capacitor (SC) circuits used for DT operation. However, RF sampling may also offer advantages on the compatibility to CMOS

[4]On the other hand, a "hold effect" can provide DT-to-CT conversion, e.g., used as the reconstruction filter in a digital-to-analog converter. Effectively a hold increases the observation rate from finite (DT) to infinite (CT). Interestingly, applying a hold following a sampler, which makes a sample-and-hold (S/H) together, introduces a coefficient proportional to the holding time, which may also cancel the factor $1/T_s$ in (1).

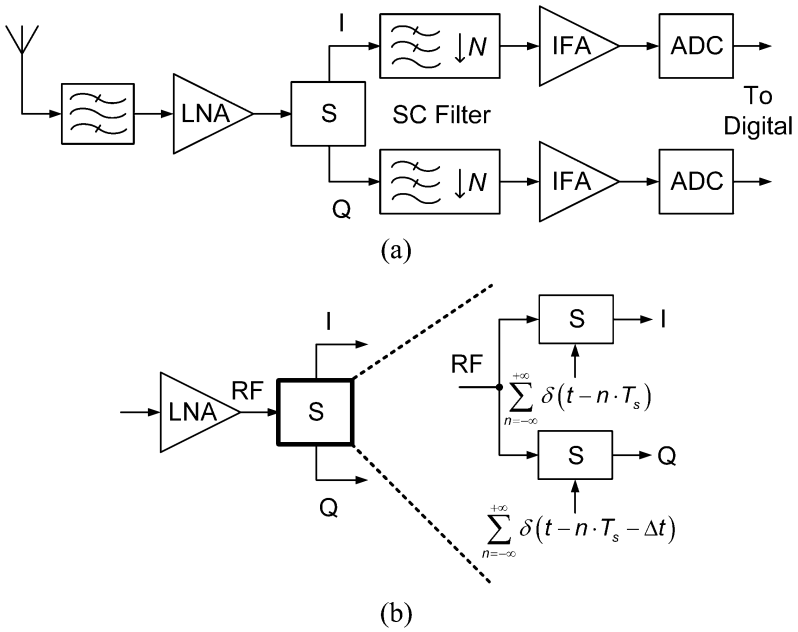

Fig. 3. (a) Block diagram of a traditional RF-sampling receiver; (b) Traditional RF-sampling receiver using a time delay Δt for quadrature demodulation.

scaling [3]–[6], [23] and system-on-chip (SoC) integration [4], [5], for instance, by extensively using of switches, capacitors and timing. Switching speed is a MOS device performance indicator that steadily improves with technology scaling [6]. The baseband selectivity is digitally controlled by the clock frequency and the capacitance ratio, both of which can be very precise in deep-sub-micron CMOS [3] and therefore be robust to process variation and improve the yield. Migration from one CMOS process node to the next may also be easier [4]. As CMOS continues scaling and the SoC trend goes on, it seems worthwhile to explore the potential of building a SDR receiver based on RF-sampling techniques.

We will now focus on an RF-sampling receiver exploiting the DT-mixing architecture as sketched in Fig. 2(b), and show how it makes RF sampling more suitable to SDR receivers.

III. Discrete-Time Mixing Receiver Architecture

Fig. 3(a) shows a traditional RF-sampling receiver, consisting of an RF pre-select filter, LNA, RF sampler, a chain of SC-circuits for filtering and decimation, IF amplifier (IFA), and ADC. However, the traditional RF-sampling receivers face a few challenges when applied to SDR, including 1) the narrowband quadrature demodulation and 2) the noise and interference folding due to aliasing. We will propose an architecture-level solution, namely DT mixing, which allows both wideband quadrature demodulation and wideband harmonic rejection to reduce aliasing. This differs from traditional RF-sampling receivers, which realize downconversion via CT-to-DT sampling or DT re-sampling. Next, we will address the two challenges mentioned above.

A. DT Mixing Concept and Wideband Quadrature Demodulation

Known RF-sampling receivers often use "second-order sampling" [24]: a time delay Δt between the two sampling paths approximates a desired phase shift, e.g., 90° for I/Q demodulation, as shown in Fig. 3(b). The resulted phase shift $\Delta\varphi$ between I and Q at IF is given by [12, Section III][5]

$$\Delta\varphi = 2\pi \cdot f_{\mathrm{RF}} \cdot \Delta t \tag{4}$$

where f_{RF} is the frequency of the RF input signal (not the center frequency). Thus, the desired exact $\Delta\varphi$ is only obtained at specific RF-frequencies, e.g., for 90° only frequencies of $\{(k + 0.25)/\Delta t\}$ where k is an integer.

Usually Δt is chosen in such a way that the phase shift is exact for the center frequency (f_c) of the desired RF signal. Rearranging (4), and substituting $\Delta\varphi = \pi/2 + k\cdot 2\pi$, the following condition holds:

$$\Delta t = \frac{\pi/2 + k \cdot 2\pi}{2\pi f_c} = \frac{k + 0.25}{f_c}. \tag{5}$$

The absolute phase error at (arbitrary) frequency f_{RF} then is

$$|\varphi_e| = |2\pi \cdot (f_{\mathrm{RF}} - f_c) \cdot \Delta t|. \tag{6}$$

In contrast, the phase shift generated by a CT-mixing receiver can be written as $\Delta\varphi = 2\pi\cdot f_{\mathrm{LO}}\cdot\Delta t$, which is proportional to the *LO frequency* (f_{LO}) instead of f_{RF}. If $\Delta t = 1/(4f_{\mathrm{LO}})$, $\Delta\varphi$ can be constantly 90° over any f_{RF}. Hence, there is no systematic I/Q phase error for CT-mixing.

Larger phase error leads to less accurate quadrature demodulation and degraded image rejection. From (6), we can see the maximum phase error is proportional to the channel BW which is $2 \cdot |f_{\mathrm{RF,max}} - f_c|$ for a zero-IF receiver, and the time delay Δt which is inversely proportional to f_c according to (5). Note that the sampling frequency (f_s) does not determine the phase error. For the smallest $|\varphi_e|$, we need the smallest time delay, i.e.,

[5]To assist the understanding, here we correct two printing errors during the PDF conversion in [12]: a) just above Fig. 2 of [12], "$0 \cdot \Delta t < T_s$" should be "$0 \le \Delta t < T_s$"; b) in the third line below Fig. 3 of [12], "$(t - nT_s - \Delta t)$" should be "$\Sigma\delta(t - n \cdot T_s - \Delta t)$".

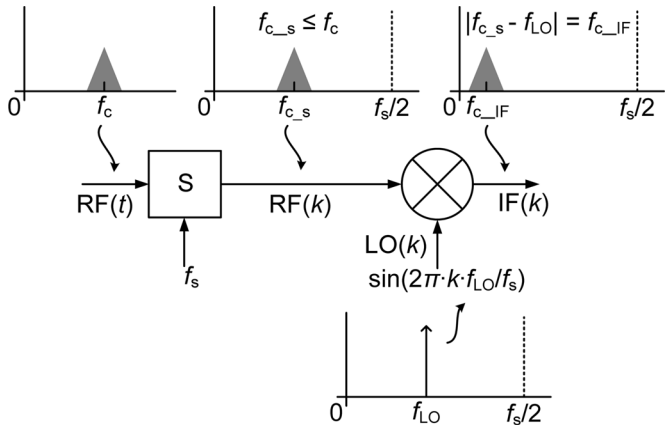

Fig. 4. A basic discrete-time mixing downconverter.

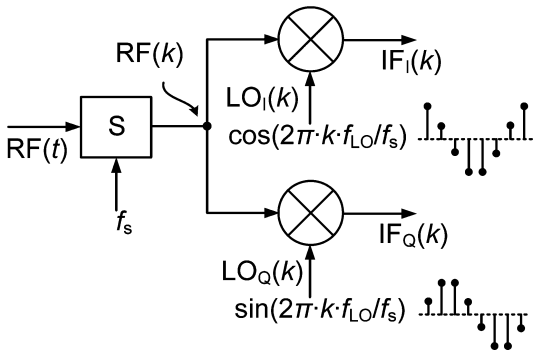

Fig. 5. A discrete-time (DT) mixing downconverter using I/Q DT mixers.

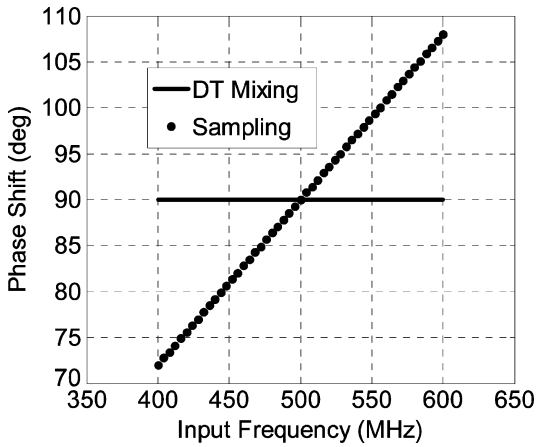

Fig. 6. Simulated phase difference between the I and Q IF-signals as a function of the input RF at a center frequency of 500 MHz, showing mixing has benefits in maintaining 90 degrees over a wide band.

$k = 0$ so $\Delta t = 0.25/f_c$. At GHz frequencies (f_c) and a few MHz channel BW, the error can still be acceptable without correction, but for lower f_c or larger channel BW it easily becomes several degrees. For example, for ultra-wideband applications, a 528 MHz channel around a 3.432 GHz carrier in a zero-IF receiver leads to $f_c = 3.432$ GHz and $|f_{\mathrm{RF,max}} - f_c| = 264$ MHz. According to (6) considering $\Delta t = 0.25/f_c$, it means a maximum phase error of 7°. For SDR applications which are aimed to accommodate any standards, such phase error is undesired.

Since the phase error can be predicted as (6), it should be possible to compensate it in the digital domain [25] at the cost of extra power and complexity. On the other hand, the *phase shift introduced by mixing is theoretically constant over frequency* since the multiplication operation conveys the phase from the LO to the IF signal. We propose to retain this favorable property of mixing in an RF-sampling receiver, via a DT-mixing architecture.

The basic DT-mixing downconverter is shown in Fig. 4, consisting of a sampler followed by a DT mixer. Now we explain its general working principle. The sampler running at f_s converts the RF input signal centered at f_c from CT to DT domain, i.e., RF(t) to RF(k). In principle, there is no specific requirement on the ratio of f_s/f_c, i.e., subsampling, Nyquist sampling and oversampling are all possible. Assume the sampled signal RF(k) has a center frequency of f_{c_s} and is sampled at a rate of f_s, where $f_{c\_s} \le f_c$ holds as a result of sampling. In the DT mixer the signal RF(k) is mixed with a DT sine-wave LO(k) of frequency f_{LO} and also sampled at f_s. The IF output signal IF(k) is centered at f_{c_IF} (see Fig. 4) and the relationship $f_{c\_\mathrm{IF}} = |f_{c\_s} - f_{\mathrm{LO}}|$ holds as a result of mixing downconversion. Note that downconversion may happen in both the sampler and the DT mixer stages.

For I/Q DT mixing, as shown in Fig. 5, a single sampling stage converts a CT signal RF(t) into the DT domain, followed by two DT mixers multiplying the sampled signal RF(k) with a DT cosine-wave $\mathrm{LO}_I(k)$ and a DT sine-wave $\mathrm{LO}_Q(k)$ respectively. For zero-IF downconversion, the DT cosine or sine frequency f_{LO} is the same as the sampled signal center frequency f_{c_s}, i.e., $f_{\mathrm{LO}} = f_{c\_s}$. The DT cosine and sine waves have a 90° phase difference, transferred to IF via multiplication, similar to what a CT mixer does. Thus, the phase shift via DT mixing is frequency independent.

We did simulation to prove the different effects on I/Q phase shift by a traditional CT-to-DT sampling technique [Fig. 3(b)] and our proposed DT-mixing technique (Fig. 5). For both cases, we used ideal components, e.g., ideal switches and capacitors. The RF input signal is centered at 500 MHz with a 200 MHz BW and the output is at zero-IF. The phase difference between the I and Q outputs are plotted in Fig. 6, showing almost a 20° error for the traditional sampling approach, as predicted by (6), while maintaining wideband constant 90° for DT mixing.

B. Wideband Harmonic Rejection

Another challenge of an RF-sampling receiver is aliasing, as noise and interference around harmonics of the sampling frequency are folded to baseband during the sampling process. For narrowband applications, a dedicated RF filter can help [Fig. 3(a)], but for SDR applications such a filter limits the flexibility. Other solutions are desired to at least relax the requirements on the RF filter.

For a CT mixer, it is well known that all even-order harmonics can be rejected by applying differential LO signals. Moreover, in [26], a harmonic-rejection (HR) technique for CT mixers in a transmitter was proposed to suppress some odd-order harmonics. CT HR mixers have been applied for digital TV applications [27], [28]. Using a sum of weighted multi-phase square-wave clocks, an effective LO with reduced harmonic content

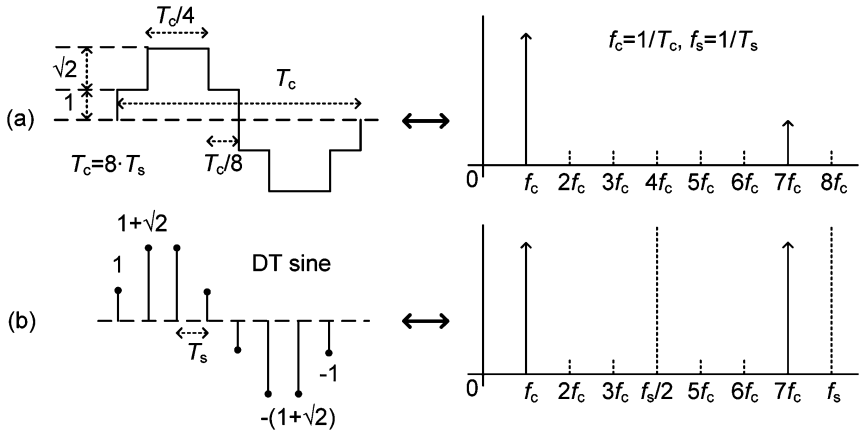

Fig. 7. Effective LO waveform for 2nd to 6th harmonic rejection and the corresponding spectrum: (a) continuous-time; (b) discrete-time.

is created (see Fig. 7). In general, the number of rejected harmonics is limited by the number of available clock phases. For example, as shown in Fig. 7(a), an effective LO summed from three $T_c/8$-time-shifted square-waves with an amplitude ratio of $1:\sqrt{2}:1$ is free of the 2nd to 6th harmonics, and only contains the $(8n \pm 1)$th harmonics ($n = 0, 1, 2\ldots$ so only 1st, 7th, 9th, etc.).

A similar idea can be applied to the DT mixers to reject sampling aliases (harmonics). Since the DT sine-wave has sampling aliases located at $(n \cdot f_s \pm f_{\rm IF})$, high sample rate reduces the amount of in-band aliases (for a given RF-filter BW). So *oversampling* ($f_s > 2f_{\rm RF}$) is more effective. For zero-IF downconversion, we can choose $f_s = m \cdot f_c (m = 1, 2, 3\ldots)$. The remaining harmonics causing aliasing are the $(m \cdot n \pm 1)$th, and the first un-wanted harmonic is the $(m-1)$th. The further-away the first unwanted harmonic, i.e., a larger m, the less requirements on the RF filter. Fig. 7(b) shows an example of the DT sine-wave with $m = 8$, corresponding to Fig. 7(a).

A FIR filter in the signal path can in principle also reject sampling aliases by positioning the filter notches at the targeted antialias frequencies [29]. However, it is only effective for a limited channel BW due to the limited notch BW intrinsic to any FIR filter. Alternatively, the stop-band of a FIR filter could also reduce harmonic interferers, where the rejection bandwidth is limited by the pass-band and the stop-band frequencies. To achieve relatively wideband rejection and a good rejection ratio, the required filter order and filter coefficients are often too complicated to be practical for an analog-DT implementation.

For SDR applications, any useful channel BW should be accommodated, so a good HR ratio over a wide channel BW is important. Wideband HR is also important to reduce the co-channel distortion caused by strong wideband interferers around harmonic frequencies even if these interferers do not directly overlap with the desired channel at baseband. Therefore, a FIR-filter based HR technique does not suit SDR applications. In contrast, the DT-mixing based HR technique does not have intrinsic channel BW limitations, i.e., it presents wideband HR, as for a CT mixer.

Besides improving signal-to-interference ratio, oversampling and harmonic rejection in a sampling receiver will also improve signal-to-noise ratio (or equivalently NF) since the noise folding is also reduced, in the same way as rejecting interference.

Summarizing, we proposed an alternative receiver architecture using RF sampling followed by DT mixing with a sampled cosine or sine wave. It enables wideband quadrature demodulation and wideband harmonic rejection, making RF sampling more suitable for SDR receivers.

IV. Proof-of-Concept Implementation

To prove the concept of DT mixing, we implemented a prototype receiver to cover 0.2 to 0.9 GHz RF range, targeting the CR applications recently proposed in the television broadcasting band [14]. The wideband features of DT mixing can be useful for CR applications which might use non-contiguous segments of free spectrum distributed over a wide band.

A. Receiver Architecture

Fig. 8 shows the architecture of the receiver. For clarity it is shown single-ended, but in fact all circuits are implemented differentially. Please note that the LNA is not included in this work, but is included in [15]. An inverter-based RF voltage amplifier (RFA) delivering 6dB gain drives a passive switched-capacitor (SC) core consisting of three stages. The first stage is effectively an oversampler (S), with a sample rate 8 times the input center frequency, i.e., $f_s = 8f_c$, for 2nd to 6th harmonic rejection [Fig. 7(b)]. The second stage consists of I/Q DT mixers for downconversion to zero-IF ($f_{\rm LO} = f_c$). The third stage is a low-pass IIR filter (LP IIR), removing undesired interference and serving as an antialiasing filter before decimation to lower sample rate. For measurement purpose, the quadrature IF outputs are buffered via source-followers (B) with a voltage gain of 1. An on-chip clock generator, consisting of clock buffer (CB), divide-by-4, and 1/8-duty-cycle driver, controls the SC core.

Fig. 9 illustrates how this DT HR mixer works. The I/Q DT mixers shown in Fig. 8 multiply the incoming samples with DT cosine and sine waves, i.e., weighting ratio of $1:(1+\sqrt{2})$ if cosine and sine waves with frequency f_c are sampled at $8f_c$. Since the DT clock is periodic with $f_{\rm LO} = f_c$, its spectrum only contains an impulse at f_c within the DC to $f_s/2$ range. Multiplying the oversampled signal with the DT clock will down-convert

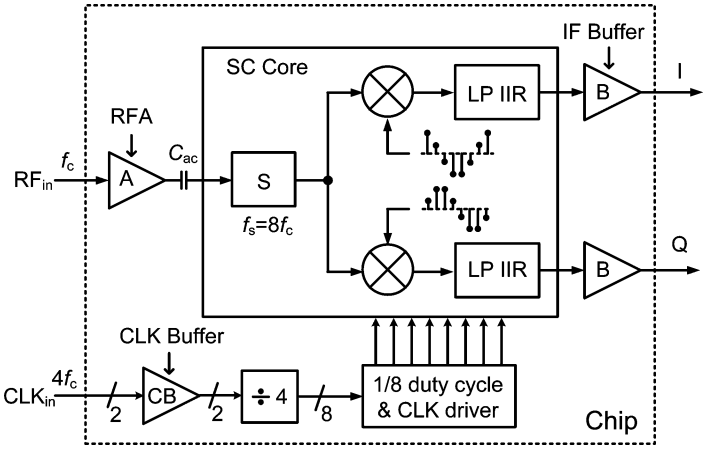

Fig. 8. Block diagram of the implemented DT-mixing receiver with 8 times oversampling and 2nd-to-6th harmonic rejection.

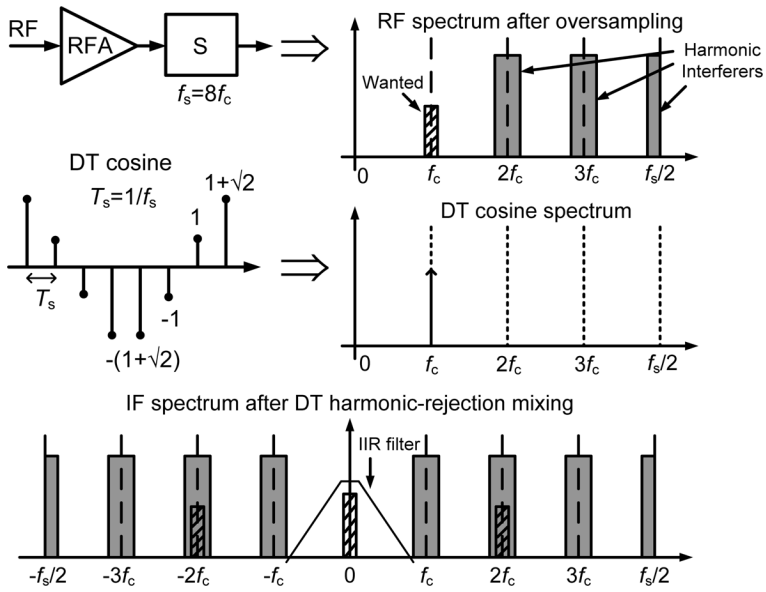

Fig. 9. Mechanism of the discrete-time (DT) harmonic-rejection mixing.

the signal from f_c to DC without folding harmonics at $2f_c$, $3f_c$, and $4f_c$. However, the harmonics already folded to f_c during the sampling process cannot be differentiated from the wanted signal. Since $f_s = 8f_c$, during sampling, the 7th harmonic folds to f_c, and the 5th harmonic folds to $3f_c$, etc. Therefore, the un-suppressed RF harmonics are the 7th, 9th, 15th, 17th etc, but the close-by 3rd and 5th and all even-order harmonics are removed. Mixing with the DT cosine and sine waves also leads to a true frequency-independent 90° phase shift for wideband quadrature demodulation.

To better understand the implementation, a more detailed description for some of the key blocks will follow.

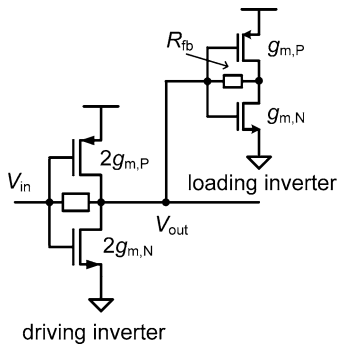

Fig. 10. The schematic of RFA based on inverters.

B. Circuit Implementation

1) RFA: The RFA is shown in Fig. 10, which is single-ended and consists of two inverters. Two copies of such an RFA are employed for differential operation. For a gain of two, the driving inverter, with a large feedback resistor for automatic DC bias, is twice the size of the loading inverter, with a small feedback resistor R_{fb} around $2/(g_{m,P} + g_{m,N})$ to partially compensate the 3rd-order nonlinearity [15]. Nominally, the driving inverter draws 1mA with a total g_m of 20 mS and the loading inverter takes 0.5 mA with 10 mS.

Please note that the RFA is not a complete LNA and its input is not matched to 50 Ω but targeted at high impedance. Functionally the RFA is not required for realizing the DT mixing

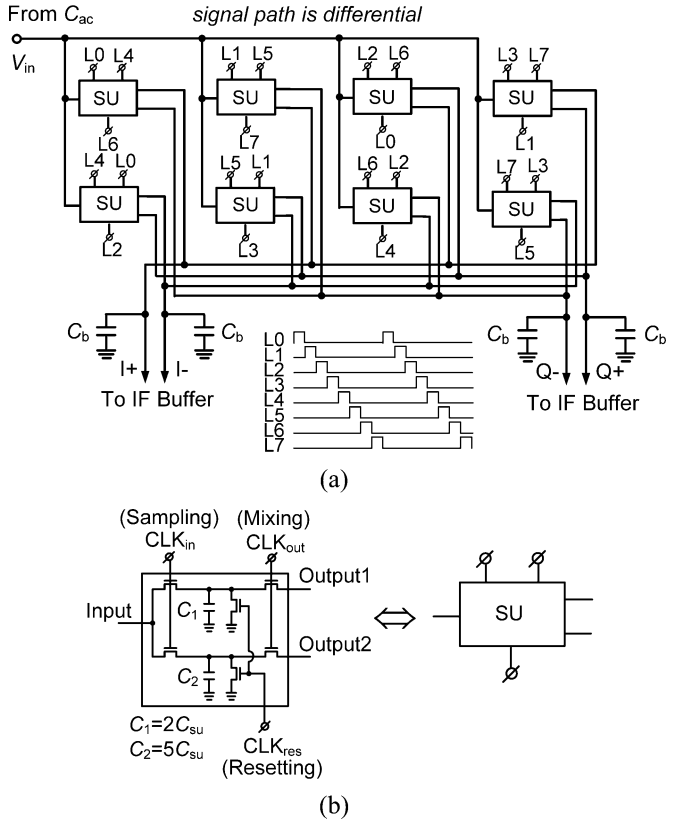

Fig. 11. (a) Switched-capacitor (SC) core circuitry with 8-phase clock waveform. (b) Transistor-level construction of a sampling unit (SU).

concept. It mainly serves as a buffer to drive the follow-up SC circuitry for measurement purposes. Without a buffer, the input impedance of a SC chip is more complicated, which can depend on the driving source impedance [19].

2) SC Core: Fig. 11(a) shows the SC core circuitry. In total, there are 16 sampling units (SU) implemented, but for clarity only half of the differential system is shown. An AC coupling capacitor ($C_{ac} = 2.5$ pF) is used between RFA and the SC core input as shown in Fig. 8, so that the sampling units can work at a common-mode (CM) level of ground (GND), which is defined by reset switches inside the sampling units [see Fig. 11(b)]. The clock (L0-L7) swings from GND to VDD to minimize the switch-on resistance of nMOS switches, for a good linearity and a small time constant. The clock design also aims at a fast falling edge to reduce distortion introduced at the sampling moment. Four buffer capacitors C_b (18 pF each) are used to store the signal charge for quadrature outputs, built via nMOS accumulation capacitors for small area.

Fig. 11(b) shows a sampling unit in detail. In each SU, there are two weighted sampling capacitors to map the $1:(1+\sqrt{2})$ weighted pulse amplitudes needed for a DT cosine or sine wave. In previous work, weighted amplifiers were used [9], [26]–[29]. We exploit weighted capacitors (C_1, C_2) which can have superior matching properties for good amplitude (weighting factor) accuracy in HR. To make a non-integer $1:(1+\sqrt{2})$ ratio reliable in layout is difficult. We used unit capacitors with value C_{su} in a 2:5 ratio as approximation ($C_1 = 2C_{su} = 160$ fF, $C_2 = 5C_{su} = 400$ fF), built via metal–oxide–metal (MOM) capacitors for high linearity. In each SU, there are three pairs of switches controlled by three different clock phases, and in each pair the two switches also share the same weighting factor as the two capacitors. The switch pair for sampling ("sampling switches") is controlled by $\mathrm{CLK_{in}}$, and the switch pair for DT mixing ("mixing switches") is controlled by $\mathrm{CLK_{out}}$. The third switch pair for resetting ("resetting switches") controlled by $\mathrm{CLK_{res}}$ defines the CM level of all switches to GND.

The working procedure of a SU is as follows, taking the upper left unit in Fig. 11(a) as an example:

1) at clock phase L0 ($\mathrm{CLK_{in}}$ high), the sampling switches take the same RF voltage to two sampling capacitors C_1 and C_2;
2) then the charge will be kept for three idle phases, and at phase L4 ($\mathrm{CLK_{out}}$ high) the two charge samples will be transferred via the "mixing switches" to two buffer capacitors C_b, one in I path (I+ side) and the other in Q path (Q- side);
3) waiting for another idle phase, in phase L6 ($\mathrm{CLK_{res}}$ high) the reset switches clean up the sampling capacitors C_1 and C_2;
4) and after one more idle phase, the whole procedure repeats from phase L0.

The other 7 units experience the same pattern of activity but shifted in time. By inserting some idle phases between each operation (sampling, mixing, or resetting), we can guarantee the three switching operations do not disturb each other during the phase transitions.

Next we will describe each functional blocks, i.e., the sampler, the DT mixer, and the IIR filter, in the SC core of Fig. 8.

a) Sampler: We aim for a voltage sampler, to reduce the frequency dependency of conversion gain [12], although it suffers from noise folding. Oversampling can reduce the noise folding and hence improve NF. The oversampling function is implemented via a time-interleaved sampling structure. Eight interleaved sampling units are controlled by 8-phase non-overlapping clocks with 1/8 duty cycle, as shown in Fig. 11(a). Each of the 8-phase clocks gives a sample rate of f_c, so 8-times interleaving results in an effective sample rate of $8f_c$. Using time-interleaved sampling to achieve oversampling, there is no extra cost on clock speed compared to other HR systems [9], [26]–[29], where multiphase clocks are also employed. Note that achieving 8-times oversampling only requires doubled clock speed compared to what is needed for regular quadrature downconversion, where 4-phase clock is used.

The switch size is selected so that the switch-on resistor and the sampling capacitor forms a relatively small time constant $\tau = 20$ ps. Since the targeted upper input center frequency (f_c) is 900 MHz and the clock duty cycle is 1/8, the minimum switch-on time per period is 139 ps, which corresponds to 7τ and guarantees small voltage signal attenuation [30].

b) DT Mixer: The DT mixing is implemented in the charge domain, via a systematic combination of the mixing switches from all SUs to transfer the charge samples from the sampling capacitors (C_1,C_2) to the buffer capacitors (C_b). Effectively the DT mixing is realized via *de-multiplexing* as shown in Fig. 12. The oversampled charge data stream RF(k) goes through the switching network controlled by $\mathrm{CLK_{out}}$ in Fig. 11(b) and becomes IF(k). For illustration, Fig. 12 actually

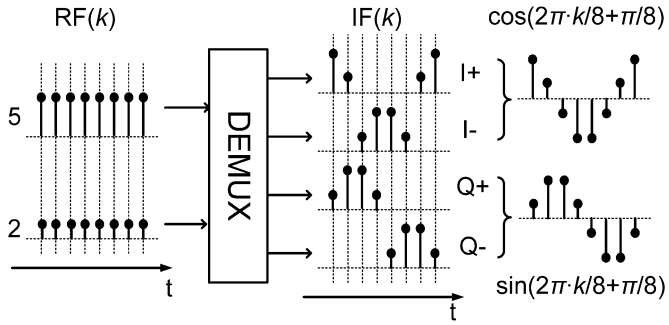

Fig. 12. To implement discrete-time mixing via de-multiplexing.

Initial Phase	0	π/8
I	cos(2π·k/8)	cos(2π·k/8+π/8)
Q	sin(2π·k/8)	sin(2π·k/8+π/8)
|I|+|Q|	≠constant	=constant
	Extra dummy Needed	*Identical loading to each clock phase*

Fig. 13. Comparison of two initial phase choices for the DT cosine and sine: $\pi/8$ is preferred.

shows an example with a DC input RF(k) which is up-converted to become a quadrature DT sinusoidal output IF(k). But the same principle applies to downconversion. Note that the DT-cosine or DT-sine also has a sample rate of $8f_c$ but the frequency of the DT cosine-wave or DT sine-wave is f_c, as illustrated in Figs. 7(b) and 9.

Changing the initial phase of the DT cosine and sine, the resulting LO waveform can be different, leading to a different ratio among sampling capacitors. As shown in Fig. 13, by choosing the initial phase to be $\pi/8$, we have

$$|\cos(2\pi \cdot k/8 + \pi/8)| + |\sin(2\pi \cdot k/8 + \pi/8)| = \text{constant}. \tag{7}$$

This choice guarantees the identical loading for all clock phases without extra dummy needed. The identical loading for each clock phase is important for both gain and phase accuracies.

Conversion gain (CG) is an important parameter of mixer. In general, the systematic CG of a DT mixer can be derived [31] as

$$CG = \frac{1}{2}\left(\sum_{i=1}^{n}|p_i| \Big/ n\right)^{-1}. \tag{8}$$

In (8), the "n" is the ratio of the sampling frequency to the DT sine-wave frequency ($n = f_s/f_{\rm LO}$), so that $n/2$ is the oversampling ratio. In another way of interpreting, the "n" is the total number of discrete time points in one period of the DT sine-wave, and each discrete time point has a weighting factor for its relative amplitude. The "p_i" is the value of one of the weighting factors in the DT sine-wave ($i = 1, 2, \ldots, n$). There is a "1/2" factor in (8) since the output signal amplitude at the difference frequency is halved compared to the input, just like in a CT mixing. The periodic DT sine-wave can be described by a vector $p = [p_1, p_2, \ldots, p_n]$. For example, in Fig. 13, for the DT sine-wave with an initial phase of $\pi/8$, its $n = 8$ and its $p_i = \sin[2\pi \cdot (i-1)/8 + \pi/8]$, i.e., $p = [0.38, 0.92, 0.92, 0.38, -0.38, -0.92, -0.92, -0.38]$. According to (8), the CG for such a DT mixer is 0.77.

To verify the systematic CG, we rebuild and simulate the schematic of Fig. 11(a) using ideal switches and capacitors to eliminate parasitic effects which are not considered in (8) and without applying RFA and C_{ac}. The result of -2.3 dB fits exactly what we derived above, i.e., 0.77. The overall gain of the receiver should consider the cascaded gain of RFA (6 dB), voltage sampler (0 dB), DT mixer (-2.3 dB), IIR filter (0 dB), and IF buffer (0 dB), which is then equal to $6 - 2.3 = 3.7$ dB, without considering 2nd-order effects such as parasitic capacitance.

c) IIR Filter: The charge sharing operation, between the sampling and the buffer capacitors, implements a low-pass IIR filter [3], [23]. The voltage transfer function of this IIR filter can be written as

$$H_{IIR}(Z) = \frac{1-\beta}{1-\beta \cdot Z^{-1}}; \quad \left\{\beta \approx \frac{1}{2}\left(\frac{C_b}{C_b + C_1} + \frac{C_b}{C_b + C_2}\right)\right\}. \tag{9}$$

According to (9), the IIR filter has a voltage gain of 1 at DC. The effective factor β is an average of these two charge transfer functions $F_1 = C_b/(C_b + C_1)$ and $F_2 = C_b/(C_b + C_2)$. Equivalently, β can be written as $C_b/(C_b + C_{IIR})$ and the IIR filter sees an effective sampling capacitor $C_{IIR} \approx (C_1 + C_2)/2$, if $C_1 \ll C_b$ and $C_2 \ll C_b$.

The IIR filter BW is determined by the sample rate f_s and the coefficient β. The clock frequency can be very accurate and therefore f_s can be accurate. As seen from β, the BW is defined by the capacitor-ratios which can be robust to process variation if the same type of capacitor is used. The matching between C_b and C_1 (or C_2) affects the IIR filter BW. However, since the IIR filter is not the focus of this work, a MOS accumulation capacitor was chosen for C_b to save chip area.

As an intrinsic property of DT filters, its BW scales with the sample rate f_s. To accommodate the 5 to 8 MHz channel spacing used in the television band for the CR applications [14], the -3 dB BW of this IIR filter is designed to be roughly 10 MHz when $f_c = 0.5$ GHz (or equivalently $f_s = 4$ GHz), which is around the middle of the 0.2 G–0.9 GHz band. In simulation, the -3 dB BW is 4.4 MHz at 0.2 GHz LO and 16.9 MHz at 0.9 GHz LO. Normally an IF filter BW that scales with f_s is undesired. But this effect can be compensated via a bank of selectable C_b values to adapt β to different f_s [4], [6].

A coarse noise analysis for the IIR filter can be made for Fig. 11(b), viewing the combination of the sampling switch, the sampling capacitor (C_1 or C_2), and the mixing switch as a

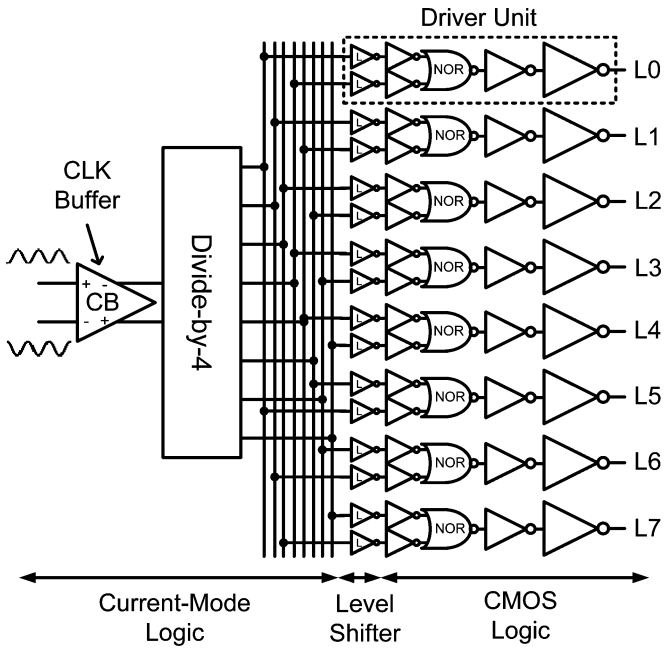

Fig. 14. Block diagram of the 8-phase clock generator.

switched-capacitor resistor, R_{sc}. Then the IIR filter can be seen as a low-pass filter formed by R_{sc} and C_b. The total integrated noise (V_n^2) after IIR filtering is KT/C$_b$. To improve the noise at constant filter BW, both C_b and C_1 & C_2 should be scaled up simultaneously.

Besides implementing the IIR filter, the charge sharing operation also shifts the amplitude ratio away from C_1: $C_2 = 2:5$, depending on the charge transfer functions F_1 and F_2. Considering $C_b = 18$ pF, $C_1 = 160$ fF, and $C_2 = 400$ fF, the effective amplitude ratio is

$$(C_1 \cdot F_1) : (C_2 \cdot F_2) = \left(C_1 \cdot \frac{C_b}{C_b + C_1}\right) : \left(C_2 \cdot \frac{C_b}{C_b + C_2}\right) \approx 1 : 2.467. \quad (10)$$

Compared to the desired $1 : (1 + \sqrt{2})$ ratio, the gain error is reduced from 3.6% (2:5 ratio) to 2.2% (1:2.467).

To reduce the sample rate operated by ADC, the outputs of IIR filter can be decimated, e.g., via a moving average, to a lower sample rate and the next stages can use further DT signal processing, e.g., FIR/IIR filter and decimation [3]–[6]. The ADC can work in DT domain, e.g., a DT $\Sigma\Delta$ ADC was used for Bluetooth [3] or for GSM [32] and a DT successive-approximation ADC for Wi-Fi/WiMax [6]. Alternatively, the ADC can also work in CT domain when the baseband sample rate is high enough and the CT filters can remove high-frequency images, e.g., a CT $\Sigma\Delta$ ADC for GSM/GPRS [4].

3) 8-Phase Clock Generator: We need 8-phase clocks to drive the SC core described above. Such a clock generator is shown in Fig. 14. It can be partitioned into three parts, namely a high-frequency current-mode logic (CML) part, a level shifter, and a CMOS logic part. The CMOS logic works with full-swing signals while the CML does not, and the level shifter bridges the gap.

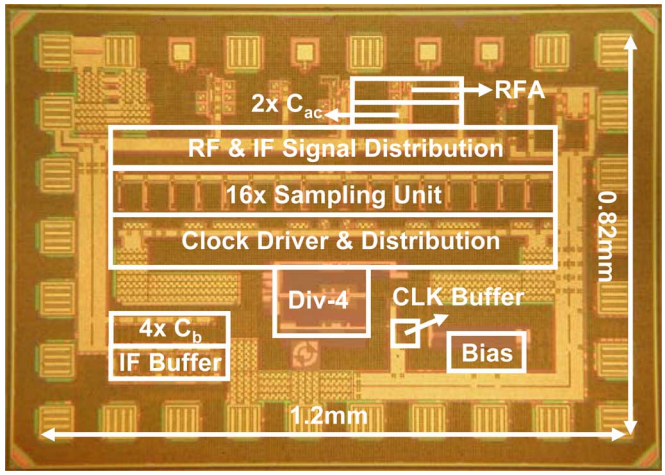

Fig. 15. Microphotograph of the chip fabricated in 65 nm CMOS with key blocks indicated.

The input receives external differential clocks at frequency $4f_c$. An nMOS CML buffer helps recover the clock steepness and reject possible common-mode interference. This buffer drives a divide-by-4 circuit consisting of four nMOS CML latches to generate 50%-duty-cycle 8-phase clocks at frequency f_c. The CML is chosen for its fully differential operation which has less effect and more immunity to the voltage supply than its CMOS counterpart.

The following stages are split into 8 paths each with a tapered driver unit. Each driver unit consists of level shifters, inverters and NOR gates to generate a 1/8-duty-cycle full-swing clock. The level shifter is simply implemented by an inverter with stronger driving capability in pMOS than in NMOS. CMOS logic is necessary at the final stages since full-swing clocks can improve both noise and linearity of the sampling circuitry by minimizing the switch-on resistance.

V. Experimental Results

Fig. 15 shows the microphotograph of the chip fabricated in a baseline 65 nm CMOS process. The active area of the chip is about 0.4 mm^2, most of which is occupied by capacitors (C_{ac}, C_{su} and C_b) and signal/clock distribution networks. The chip is packaged in a 32-pin Heat-sink Very-thin Quad Flat-pack No-leads (HVQFN) package and measured on PCB. Since the RFA input is the gate of inverter, a 100 Ω SMD resistor for impedance matching is soldered on PCB, close to the package and across the differential RF input traces. Both the receiver inputs and the clock inputs are differential and wideband hybrids (balun) were used to interface to single-ended 50 Ω measurement equipment. The IF-output voltage is sensed by a differential active probe that performs differential to single-ended conversion and impedance conversion to 50 Ω. The characteristics of all components and cables for testing are de-embedded from the results.

A. Conversion Gain and Noise Figure

Fig. 16 (left) shows the simulated[6] and measured conversion gain (CG) over the 0.2 to 0.9 GHz RF band. The results are obtained at 1 MHz IF, well within the −3 dB IF BW for the whole

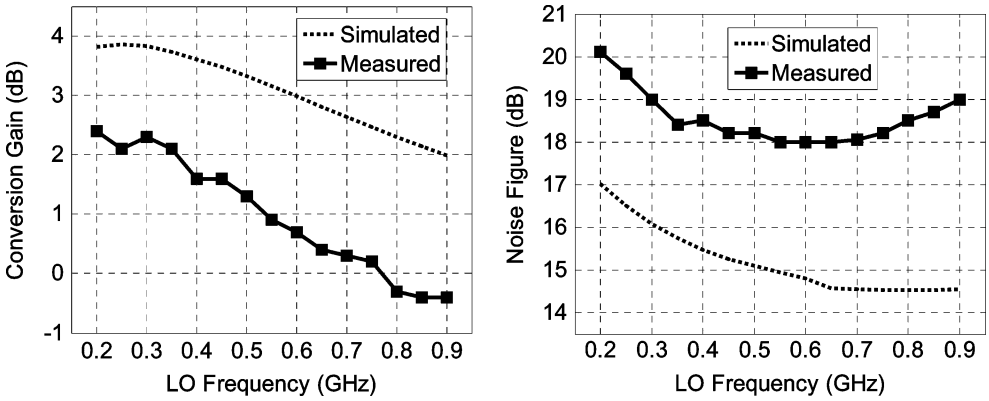

Fig. 16. Simulated and measured (on PCB) conversion gain and DSB NF versus LO frequency (IF = 1 MHz).

band. The trend of the measured gain fits well with the simulated gain. The CG drops by about 3 dB from 0.2 to 0.9 GHz, indicating the −3 dB RF BW. Analyses and simulations indicate that this strong low-pass filtering behavior is mainly due to the parasitic capacitance associated with the AC coupling capacitor C_{ac}. To improve the RF BW, the AC coupling capacitor can be moved from the signal path to the clock path, as done in [11]. In layout, long interconnecting wires between the AC coupling capacitor C_{ac} and the sampling units, as shown in Fig. 15 (RF Signal Distribution), introduce extra parasitic resistance and capacitance. Also the loss of a few centimeter PCB traces for the RF inputs was not de-embedded. These are the major causes of the gap between the simulated and measured CG.

Fig. 16 (right) presents the simulated and measured DSB NF, both referred to the matched 50 Ω source noise. Two curves show similar trend but the measured NF is about 3–4 dB worse, due to the degraded gain and the extra noise contributed by the wiring resistance for RF signal distribution (Fig. 15). Simulation shows that the SC-core contributes most noise and the additional NF contribution from the RFA is less than 1 dB. Theoretically larger gain should bring lower NF, but Fig. 16 shows an opposite trend. In fact, more noise folding at a lower sampling frequency (f_s) raises the NF, even with a higher gain, because: 1) at lower f_s the folding of switch noise is more, assuming a fixed *RC* time constant; 2) at lower f_s the folding of source noise and RFA noise is more due to the limited RF BW as indicated by the CG. Simulation shows the RFA 1/f noise has a negligible effect to the NF arise at low band. The measured NF also rises when RF is close to the upper-side limit, where the clock swing is insufficient to fully turn on the switches. As a result, less signal can pass through to IF and also the switches become noisier, so SNR is degraded at the output.

The CG and DSB NF in [13][7] were measured on wafer via probing, which showed a different trend. It's very likely due to the different way of installing the off-chip matching resistors. During wafer probing, two 50 Ω resistors for input matching were screwed on top of the probe and thus these 50 Ω resistors are further away from the chip (∼4 cm) and this will introduce a transmission-line effect leading to the trend shown in [13], as being verified by simulation. Nevertheless, since the noise from the chip is much larger than the noise from the source as indicated by the large NF, we may compare the normalized output noise (Fig. 17), via the sum of CG and NF in dB, which can get rid of the transmission-line effect and indicates mainly the circuit-generated noise at its output. Then three cases, i.e., simulated, measured on PCB and measured on wafer, show a similar trend and their discrepancy is within 1.5 dB.

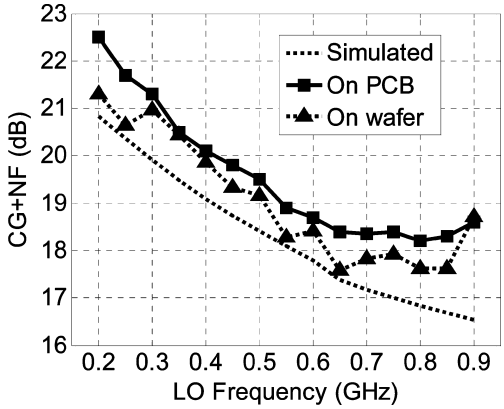

Fig. 17. Normalized output noise versus LO frequency, calculated by summing the conversion gain (CG) and noise figure (NF): simulation and measurements based on PCB and wafer probing fit better.

B. HR Ratio

Fig. 18 compares the HR ratio using two different techniques to reject harmonics: DT mixing and conventional FIR filtering [29]. As predicted by theory, the HR ratio of a sampling downconverter using FIR filtering drops significantly over the channel (simulation), while the proposed DT-mixing architecture gives wideband HR without channel BW limitation (both simulation and measurement). For DT mixing, the trend of measured results (one typical sample) fits well with the simulated results. However, phase and amplitude mismatches, which are not included in both simulated curves, degrade the HR ratio in measurement.

Fig. 19 shows the measured HR ratio over the RF band of 10 samples. The worst case 3rd and 5th HR ratios are around 25 dB and typically they are between 35 dB and 45 dB. To investigate

[6]All simulation results shown in this paper were carried out on schematic level, and no wire parasitics were included.

[7]The NF shown in [13] should be DSB NF instead of SSB NF.

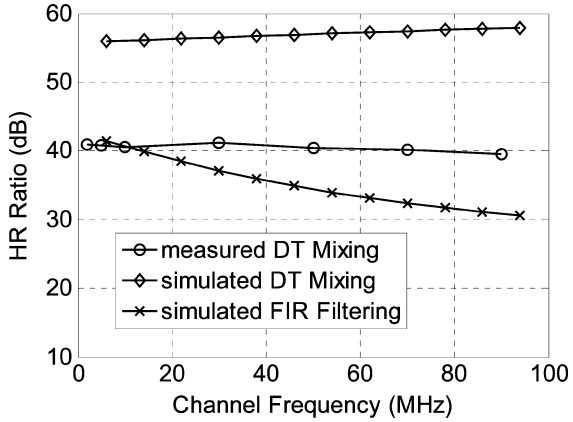

Fig. 18. Simulated (no mismatch) and measured (a typical sample with mismatch) 3rd -order harmonic-rejection (HR) ratio versus channel frequency (LO@0.5 GHz) [measured on wafer].

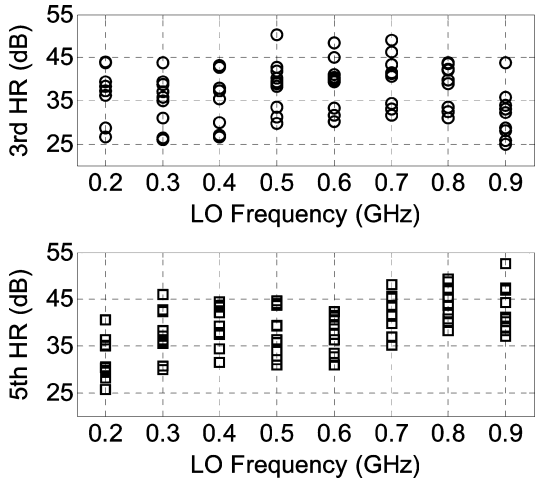

Fig. 19. Measured 3rd and 5th HR ratio versus LO frequency (10 samples) [measured on wafer].

whether phase or amplitude error is dominating, we did Monte Carlo simulations for three configurations: only amplitude error, only phase error, and both. The results are shown in Fig. 20, for 2nd to 6th harmonics of a 0.35 GHz LO. The results indicate that phase error is dominating, which affects not just the 3rd and 5th HR but also the even-order HR. We also did simulations at 0.7 GHz LO, and the same conclusion holds. The relatively large phase error is mainly due to many buffer stages used after the divider (Fig. 14), leading to large accumulated mismatch. Without using RF filters, the achieved average HR ratio of 40 dB is comparable to [9], [27], [29] showing only one chip while [28] achieves a minimum HR ratio of 40 dB. But both amplitude and phase accuracy can still be improved by techniques discussed in [11], which achieve a minimum HR ratio of 60 dB.

The HR ratios are measured with an input power of -20 dBm. When the amplitude of the harmonic interference gets bigger, both amplitude and phase accuracy of the HR mixer can be degraded. The amplitude accuracy is affected because the switch-on resistance is modulated by the instantaneous voltage of the interference. The phase accuracy is affected because the switch-on and switch-off moments are also modulated by the instantaneous voltage of the interference.

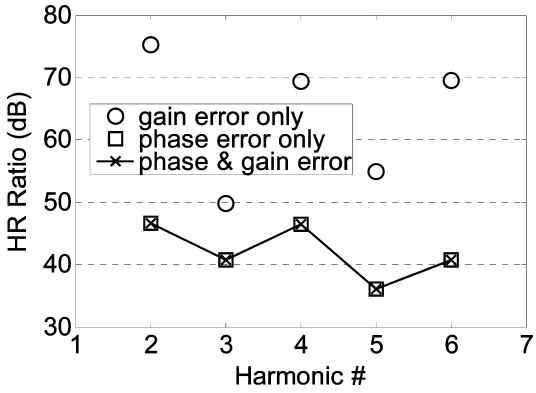

Fig. 20. Simulated 2nd to 6th HR ratio at 0.35 GHz LO (averaged in dB for 10 Monte Carlo runs, mismatch only).

TABLE II
SUMMARY OF SOME MEASURED PARAMETERS

Frequency (GHz)	0.2 to 0.9
Conv. Gain (dB)	-0.5 to 2.5
DSB NF (dB)	18 to 20
IIP3[1]	+10dBm
IIP2[1]	+53dBm
1/f noise corner	250kHz
-3dB IF BW @ 0.7GHz LO	10MHz
VDD	1.2V
DC Current	< 16mA

[1] Two tones @ 501M & 501.4MHz, LO @ 500MHz

C. Performance Summary

Table II summarizes some of the measured parameters.

For the measured in-band linearity, the IIP3 is $+10$ dBm and the IIP2 is $+53$ dBm with two tones around 500 MHz. There are three contributions to distortion: the RFA, the MOSFET switches and the IF buffer. The simulated IIP3 of only the SC core is $+26$ dBm and the simulated IIP3 of only the IF buffer is $+27$ dBm. This indicates that the measured IIP3 is dominated by the RFA whose linearity can be degraded by process spread and bondwire inductance of VDD/GND supply pins [15]. Since a balun is used in measurement, the IIP3 of each single-ended RFA should be 3 dB lower, i.e., $+7$ dBm, which fits the result derived in [15]. Comparing this IIP3 of $+10$ dBm to the IIP3 of $+11$ dBm shown in [13] (measured via wafer probing) with around 3 dB adjustment for the transmission-line effect around 500 MHz RF, we may conclude that the bondwire in a packaged chip can degrade IIP3 by around 4 dB at 500 MHz RF.

The measured -3 dB IF BW is about 10 MHz at 0.7 GHz LO, while the designed IF BW is 10 MHz at 0.5 GHz LO. Since the IIR filter BW is determined by both the sampling frequency and the capacitor ratio according to (9), the difference is likely due to the variation of the C_{su}-to-C_b ratio caused by process spread, as they are built by different types of capacitors, i.e., C_{su} via MOM capacitor and C_b via MOS capacitor. In an improved design,

using the same type of capacitors for C_{su} and C_b should be able to reduce the variation of the IF BW due to process spread.

For power consumption, the RFAs draw 2.3 mA and the IF test buffers take 2.4 mA. The current consumption of the clock is 7.8 mA at 200 MHz LO and 10.6 mA at 900 MHz LO. The overall power consumption for all blocks shown in Fig. 8 is less than 16 mA (19 mW) at 1.2 V supply.

Overall, the presented DT-mixing downconverter shows a fair performance similar to others built via the CT-mixing approach, but is realized in a different way which is expected to benefit more from process scaling (see Section II-C). The proposed DT mixing technique maintains good quadrature demodulation and harmonic rejection over a wide channel BW.

VI. Conclusion

A discrete-time mixing receiver architecture allowing wideband quadrature demodulation and wideband harmonic rejection has been presented. This makes RF sampling more suitable for software-defined radio (SDR) and cognitive radio (CR) receivers.

We showed that downconversion techniques can be classified based on: 1) the type of input signal, i.e., continuous versus discrete both in time and amplitude; and 2) the downconversion principle, i.e., mixing or sampling. Six classes of downconverters exist, five of which have been proposed before. We propose an architecture that fits in the 6th class, i.e., a DT-mixing technique that operates on continuous-amplitude but discrete-time samples which can be obtained from CT-to-DT sampling. Different from mixing, sampling always changes the "observation rate" in the time domain. The suitability of CT-mixing and RF-sampling receivers for SDR has also been discussed, arguing that both can be suitable while RF-sampling can have advantages with respect to the compatibility to CMOS downscaling and SoC integration.

The proposed DT-mixing architecture has some similar features as CT mixing. It addresses two limitations of traditional RF-sampling receivers for SDRs operating with wide channel bandwidth: 1) quadrature demodulation and 2) harmonic rejection. Simulation shows wideband 90° phase shift for quadrature demodulation without systematic channel bandwidth limitation. Oversampling and harmonic rejection relax RF pre-filtering and reduce noise and interference folding. The DT mixing concept can be realized via de-multiplexing. A proof-of-concept DT-mixing downconverter for the 0.2-to-0.9 GHz RF band employing 8-times oversampling has been built in 65 nm CMOS. It can reject the 2nd-to-6th harmonics by 40dB typically and without systematic channel bandwidth limitation.

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